



SPEC® CINT2006 Result

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Cisco Systems

SPECint®_rate2006 = 887

Cisco UCS C420 M3 (Intel Xeon E5-4610, 2.40 GHz)

SPECint_rate_base2006 = 851

CPU2006 license: 9019

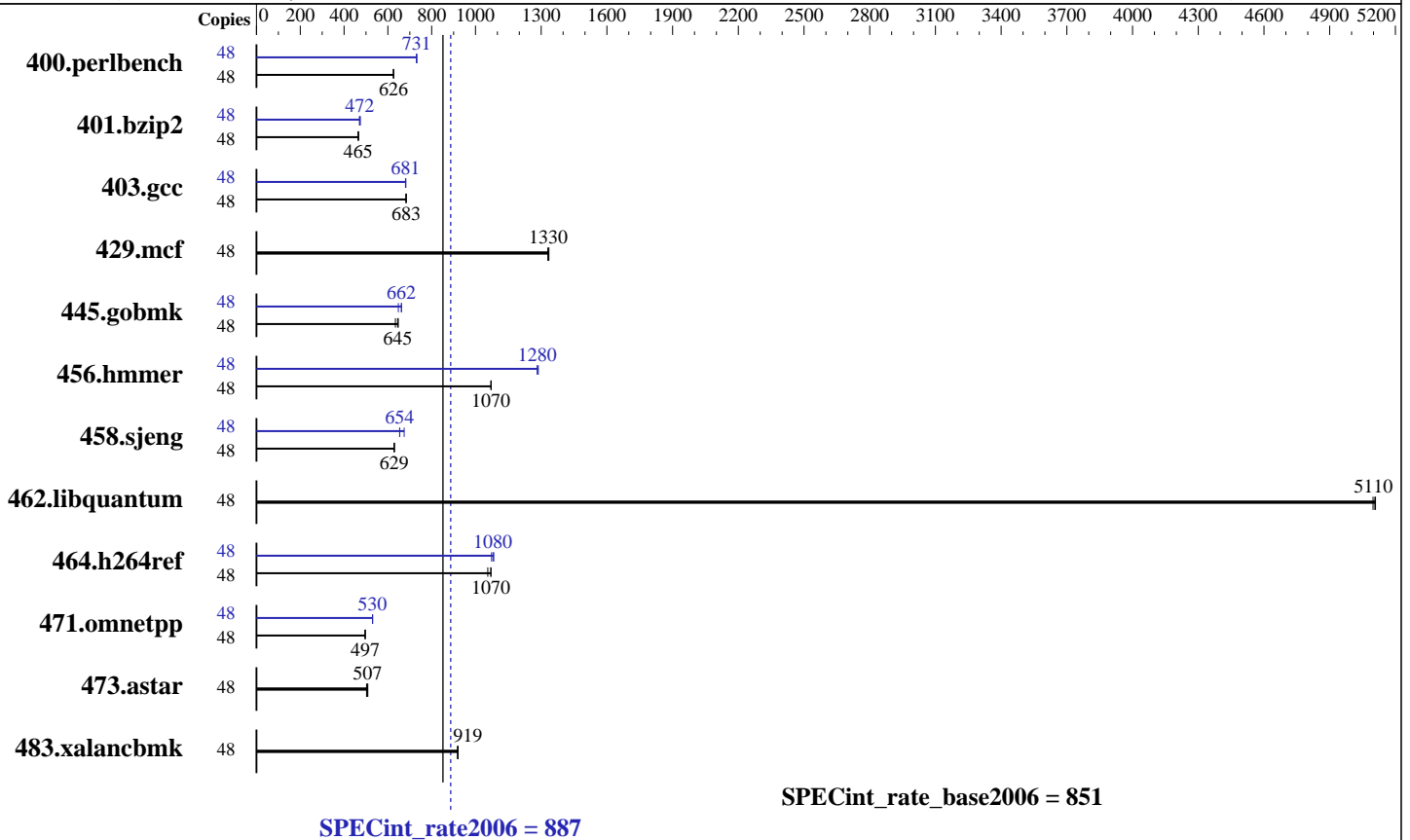
Test date: Oct-2012

Test sponsor: Cisco Systems

Hardware Availability: Sep-2012

Tested by: Cisco Systems

Software Availability: Feb-2012



Hardware

CPU Name: Intel Xeon E5-4610
 CPU Characteristics: Intel Turbo Boost Technology up to 2.90 GHz
 CPU MHz: 2400
 FPU: Integrated
 CPU(s) enabled: 24 cores, 4 chips, 6 cores/chip, 2 threads/core
 CPU(s) orderable: 1,2,3,4 chips
 Primary Cache: 32 KB I + 32 KB D on chip per core
 Secondary Cache: 256 KB I+D on chip per core
 L3 Cache: 15 MB I+D on chip per chip
 Other Cache: None
 Memory: 256 GB (32 x 8 GB 2Rx4 PC3-12800R-11, ECC, running at 1333 MHz)
 Disk Subsystem: 1 X 300 Gb 15000 RPM SAS
 Other Hardware: None

Software

Operating System: Red Hat Enterprise Linux Server release 6.2 (Santiago)
 2.6.32-220.el6.x86_64
 Compiler: C/C++: Version 12.1.3.293 of Intel C++ Studio XE for Linux
 Auto Parallel: No
 File System: ext4
 System State: Run level 3 (multi-user)
 Base Pointers: 32-bit
 Peak Pointers: 32/64-bit
 Other Software: Microquill SmartHeap V9.01



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SPECint_rate_base2006 = **851**

CPU2006 license: 9019

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Results Table

Benchmark	Base							Peak						
	Copies	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio	Copies	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio
400.perlbench	48	750	625	<u>749</u>	<u>626</u>	749	627	48	<u>642</u>	<u>731</u>	640	732	642	730
401.bzip2	48	998	464	<u>997</u>	<u>465</u>	993	466	48	977	474	986	470	<u>981</u>	<u>472</u>
403.gcc	48	<u>565</u>	<u>683</u>	565	684	566	683	48	568	680	<u>567</u>	<u>681</u>	567	682
429.mcf	48	<u>328</u>	<u>1330</u>	329	1330	328	1340	48	<u>328</u>	<u>1330</u>	329	1330	328	1340
445.gobmk	48	778	647	<u>781</u>	<u>645</u>	794	634	48	<u>761</u>	<u>662</u>	777	648	760	662
456.hammer	48	418	1070	<u>418</u>	<u>1070</u>	418	1070	48	<u>349</u>	<u>1280</u>	349	1280	348	1290
458.sjeng	48	922	630	<u>923</u>	<u>629</u>	923	629	48	861	674	889	654	<u>888</u>	<u>654</u>
462.libquantum	48	195	5100	<u>195</u>	<u>5110</u>	195	5110	48	195	5100	<u>195</u>	<u>5110</u>	195	5110
464.h264ref	48	1006	1060	<u>993</u>	<u>1070</u>	992	1070	48	<u>984</u>	<u>1080</u>	980	1080	990	1070
471.omnetpp	48	605	496	604	497	<u>604</u>	<u>497</u>	48	566	530	<u>566</u>	<u>530</u>	566	530
473.astar	48	670	503	<u>665</u>	<u>507</u>	663	508	48	670	503	<u>665</u>	<u>507</u>	663	508
483.xalancbmk	48	360	920	361	918	<u>360</u>	<u>919</u>	48	360	920	361	918	<u>360</u>	<u>919</u>

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Submit Notes

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

Platform Notes

BIOS Configuration:

Processor Power State C6 set to Disabled

Processor Power State C1 Enhanced set to Disabled

Power Technology set to Custom

Energy Performance set to Performance

DRAM Clock Throttling set to Performance

Sysinfo program /opt/cpu2006-1.2/config/sysinfo.rev6800

\$Rev: 6800 \$ \$Date:: 2011-10-11 #\$ 6f2ebdff5032aaa42e583f96b07f99d3

running on localhost.localdomain Fri Oct 12 12:11:44 2012

This section contains SUT (System Under Test) info as seen by some common utilities. To remove or add to this section, see:

<http://www.spec.org/cpu2006/Docs/config.html#sysinfo>

From /proc/cpuinfo

model name : Intel(R) Xeon(R) CPU E5-4610 0 @ 2.40GHz

4 "physical id"s (chips)

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Platform Notes (Continued)

48 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)

```
cpu cores : 6
siblings  : 12
physical 0: cores 0 1 2 3 4 5
physical 1: cores 0 1 2 3 4 5
physical 2: cores 0 1 2 3 4 5
physical 3: cores 0 1 2 3 4 5
cache size : 15360 KB
```

From /proc/meminfo

```
MemTotal:      264503292 kB
HugePages_Total: 0
Hugepagesize:  2048 kB
```

/usr/bin/lsb_release -d

```
Red Hat Enterprise Linux Server release 6.2 (Santiago)
```

From /etc/*release* /etc/*version*

```
redhat-release: Red Hat Enterprise Linux Server release 6.2 (Santiago)
system-release: Red Hat Enterprise Linux Server release 6.2 (Santiago)
system-release-cpe: cpe:/o:redhat:enterprise_linux:6server:ga:server
```

uname -a:

```
Linux localhost.localdomain 2.6.32-220.el6.x86_64 #1 SMP Wed Nov 9 08:03:13
EST 2011 x86_64 x86_64 x86_64 GNU/Linux
```

run-level 2 Oct 11 23:28

SPEC is set to: /opt/cpu2006-1.2

```
Filesystem      Type      Size  Used Avail Use% Mounted on
/dev/sda2       ext4      274G   40G  220G  16% /
```

Additional information from dmidecode:

Memory:

```
8x 0xCE00 M393B1K70DH0-YH9 8 GB 1333 MHz 2 rank
24x 0xCE00 M393B1K70DH0-YK0 8 GB 1600 MHz 2 rank
```

(End of data from sysinfo program)

General Notes

Environment variables set by runspec before the start of the run:

LD_LIBRARY_PATH = "/opt/cpu2006-1.2/libs/32:/opt/cpu2006-1.2/libs/64"

Intel HT Technology=enable

Binaries compiled on a system with 2 X Intel Xeon E5-2690 CPU + 128 GB memory using RHEL 6.2

Transparent Huge Pages enabled with:

echo always > /sys/kernel/mm/redhat_transparent_hugepage/enabled

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General Notes (Continued)

Filesystem page cache cleared with:
echo 1> /proc/sys/vm/drop_caches

Base Compiler Invocation

C benchmarks:
icc -m32

C++ benchmarks:
icpc -m32

Base Portability Flags

400.perlbench: -DSPEC_CPU_LINUX_IA32
462.libquantum: -DSPEC_CPU_LINUX
483.xalancbmk: -DSPEC_CPU_LINUX

Base Optimization Flags

C benchmarks:
-xSSE4.2 -ipo -O3 -no-prec-div -opt-prefetch -opt-mem-layout-trans=3

C++ benchmarks:
-xSSE4.2 -ipo -O3 -no-prec-div -opt-prefetch -opt-mem-layout-trans=3
-Wl,-z,muldefs -L/smartheap -lsmartheap

Base Other Flags

C benchmarks:
403.gcc: -Dalloca=_alloca

Peak Compiler Invocation

C benchmarks (except as noted below):
icc -m32

400.perlbench: icc -m64

401.bzip2: icc -m64

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Peak Compiler Invocation (Continued)

456.hmmr: icc -m64

458.sjeng: icc -m64

C++ benchmarks:

icpc -m32

Peak Portability Flags

400.perlbench: -DSPEC_CPU_LP64 -DSPEC_CPU_LINUX_X64

401.bzip2: -DSPEC_CPU_LP64

456.hmmr: -DSPEC_CPU_LP64

458.sjeng: -DSPEC_CPU_LP64

462.libquantum: -DSPEC_CPU_LINUX

483.xalancbmk: -DSPEC_CPU_LINUX

Peak Optimization Flags

C benchmarks:

400.perlbench: -xSSE4.2(pass 2) -prof-gen(pass 1) -ipo(pass 2)
-O3(pass 2) -no-prec-div(pass 2) -prof-use(pass 2)
-auto-ilp32

401.bzip2: -xSSE4.2(pass 2) -prof-gen(pass 1) -ipo(pass 2)
-O3(pass 2) -no-prec-div(pass 2) -prof-use(pass 2)
-opt-prefetch -auto-ilp32 -ansi-alias

403.gcc: -xSSE4.2 -ipo -O3 -no-prec-div

429.mcf: basepeak = yes

445.gobmk: -xSSE4.2(pass 2) -prof-gen(pass 1) -prof-use(pass 2)
-ansi-alias -opt-mem-layout-trans=3

456.hmmr: -xSSE4.2 -ipo -O3 -no-prec-div -unroll2 -auto-ilp32

458.sjeng: -xSSE4.2(pass 2) -prof-gen(pass 1) -ipo(pass 2)
-O3(pass 2) -no-prec-div(pass 2) -prof-use(pass 2)
-unroll4 -auto-ilp32

462.libquantum: basepeak = yes

464.h264ref: -xSSE4.2(pass 2) -prof-gen(pass 1) -ipo(pass 2)
-O3(pass 2) -no-prec-div(pass 2) -prof-use(pass 2)
-unroll2 -ansi-alias

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Peak Optimization Flags (Continued)

C++ benchmarks:

471.omnetpp: -xSSE4.2(pass 2) -prof-gen(pass 1) -ipo(pass 2)
-O3(pass 2) -no-prec-div(pass 2) -prof-use(pass 2)
-ansi-alias -opt-ra-region-strategy=block -Wl,-z,muldefs
-L/smartheap -lsmartheap

473.astar: basepeak = yes

483.xalancbmk: basepeak = yes

Peak Other Flags

C benchmarks:

403.gcc: -Dalloca=_alloca

The flags files that were used to format this result can be browsed at

<http://www.spec.org/cpu2006/flags/Intel-ic12.1-official-linux64.20120425.html>
<http://www.spec.org/cpu2006/flags/Cisco-Platform-Settings-V1.2.20130607.html>

You can also download the XML flags sources by saving the following links:

<http://www.spec.org/cpu2006/flags/Intel-ic12.1-official-linux64.20120425.xml>
<http://www.spec.org/cpu2006/flags/Cisco-Platform-Settings-V1.2.20130607.xml>

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For other inquiries, please contact webmaster@spec.org.

Tested with SPEC CPU2006 v1.2.
Report generated on Thu Jul 24 14:00:17 2014 by SPEC CPU2006 PS/PDF formatter v6932.
Originally published on 7 November 2012.