



SPECaccel[®]2023 Result

Copyright 2023-2024 Standard Performance Evaluation Corporation

Cisco Systems
AMD EPYC 9754
Cisco UCS C245 M8

SPECaccel2023_base = 0.8374

SPECaccel2023_peak = Not Run

accel2023 License: 9019

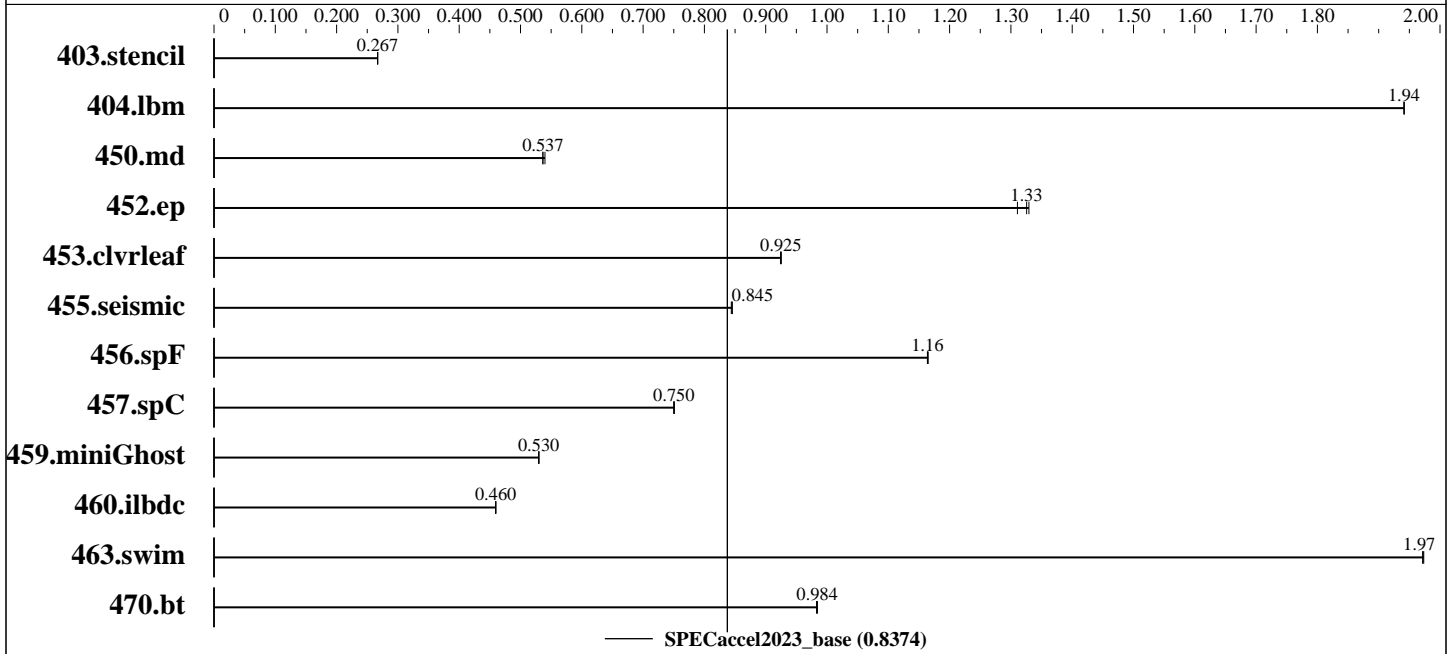
Test Sponsor: Cisco Systems

Tested by: Cisco Systems

Test Date: May-2024

Hardware Availability: Jun-2024

Software Availability: Feb-2024



Hardware

CPU Name: AMD EPYC 9754
 Max MHz.: 3100
 Nominal: 2250
 Enabled: 128 cores, 1 chip, 2 threads/core
 Orderable: 1 chip
 Cache L1: 32 KB I + 32 KB D on chip per core
 L2: 1 MB I+D on chip per core
 L3: 256 MB I+D on chip per chip,
 16 MB shared / 8 cores
 Other: None
 Memory: 768 GB (12 x 64 GB 2Rx4 PC5-5600B-R,
 running at 4800 MHz)
 Storage: 1 x 240 GB M.2 SSD
 Other: None
 Base Threads Run: 256
 Min. Peak Threads: --
 Max. Peak Threads: --

Accelerator

Accel Model Name: AMD EPYC 9754
 Accel Vendor: AMD
 Accel Name: AMD EPYC 9754
 Type of Accel: CPU
 Accel Connection: N/A
 Does Accel Use ECC: Yes
 Accel Description: 1 x AMD EPYC 9754
 Accel Driver: N/A

Software

OS: SUSE Linux Enterprise Server 15 SP5
 5.14.21-150500.53-default
 Compiler: Intel oneAPI DPC++/C++ Compiler,
 Version 2024.0.2
 Firmware: Version C245M8.4.3.4.255.0410240854 released
 Apr-2024
 File System: xfs
 System State: Run level 3 (multi-user)

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Software (Continued)

Other: None
Base Parallel Model: LOP
Base Threads Run: 256
Peak Parallel Models: Not Run
Max. Peak Threads: --
Min. Peak Threads: --

Results Table

Benchmark	Base							Peak						
	Model	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio	Model	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio
403.stencil	LOP	1649	0.267	<u>1648</u>	<u>0.267</u>	1648	0.267							
404.lbm	LOP	234	1.94	<u>234</u>	<u>1.94</u>	234	1.94							
450.md	LOP	<u>1118</u>	<u>0.537</u>	1111	0.540	1119	0.536							
452.ep	LOP	<u>313</u>	<u>1.33</u>	312	1.33	317	1.31							
453.clvleaf	LOP	1081	0.925	1082	0.924	<u>1081</u>	<u>0.925</u>							
455.seismic	LOP	922	0.846	924	0.844	<u>923</u>	<u>0.845</u>							
456.spF	LOP	408	1.16	408	1.17	<u>408</u>	<u>1.16</u>							
457.spC	LOP	719	0.751	720	0.750	<u>720</u>	<u>0.750</u>							
459.miniGhost	LOP	<u>1114</u>	<u>0.530</u>	1114	0.530	1113	0.530							
460.ilbdc	LOP	1208	0.459	1207	0.460	<u>1208</u>	<u>0.460</u>							
463.swim	LOP	223	1.97	<u>223</u>	<u>1.97</u>	223	1.97							
470.bt	LOP	<u>1072</u>	<u>0.984</u>	1073	0.983	1072	0.984							

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Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

General Notes

Environment variables set by runaccel before the start of the run:

```
FORT_BUFFERED = "true"
KMP_AFFINITY = "compact,0,granularity=thread"
KMP_BLOCKTIME = "infinite"
KMP_HW_SUBSET = "1S,128C,2T"
KMP_LIBRARY = "turnaround"
KMP_STACKSIZE = "128M"
OMP_DYNAMIC = "FALSE"
OMP_WAIT_POLICY = "active"
```

NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.

Yes: The test sponsor attests, as of date of publication, the CVE-2017-5753 (Spectre variant 1)

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General Notes (Continued)

is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

Platform Notes

Sysinfo program /home/specaccel/bin/sysinfo
Rev: r6622 of 2021-04-07 bla7d5f8f71be5aff70a755cad7211a0
running on localhost Mon May 13 01:37:05 2024

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
<https://www.spec.org/cpu2017/Docs/config.html#sysinfo>

```
From /proc/cpuinfo
model name : AMD EPYC 9754 128-Core Processor
 1 "physical id"s (chips)
256 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following
excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 128
siblings : 256
physical 0: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 28 29 30 31 32 33 34 35 36
37 38 39 40 41 42 43 44 45 46 47 48 49 50 51 52 53 54 55 56 57 58 59 60 61 62 63 64
65 66 67 68 69 70 71 72 73 74 75 76 77 78 79 80 81 82 83 84 85 86 87 88 89 90 91 92
93 94 95 96 97 98 99 100 101 102 103 104 105 106 107 108 109 110 111 112 113 114
115 116 117 118 119 120 121 122 123 124 125 126 127
```

```
From lscpu from util-linux 2.37.4:
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Address sizes: 52 bits physical, 57 bits virtual
Byte Order: Little Endian
CPU(s): 256
On-line CPU(s) list: 0-255
Vendor ID: AuthenticAMD
Model name: AMD EPYC 9754 128-Core Processor
CPU family: 25
Model: 160
Thread(s) per core: 2
Core(s) per socket: 128
Socket(s): 1
Stepping: 2
Frequency boost: enabled
CPU max MHz: 3100.3411
```

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Platform Notes (Continued)

```

CPU min MHz:                1500.0000
BogoMIPS:                    4493.21
Flags:                        fpu vme de pse tsc msr pae mce cx8 apic sep mtrr
pge mca cmov pat pse36 clflush mmx fxsr sse sse2 ht syscall nx mmxext fxsr_opt
pdpe1gb rdtscp lm constant_tsc rep_good amd_lbr_v2 nopl nonstop_tsc cpuid
extd_apicid aperfmperf rapl pni pclmulqdq monitor ssse3 fma cx16 pcid sse4_1 sse4_2
x2apic movbe popcnt aes xsave avx f16c rdrand lahf_lm cmp_legacy svm extapic
cr8_legacy abm sse4a misalignsse 3dnowprefetch osvw ibs skinit wdt tce topoext
perfctr_core perfctr_nb bpext perfctr_llc mwaitx cpb cat_l3 cdp_l3 invpcid_single
hw_pstate ssbd mba perfmon_v2 ibrs ibpb stibp vmmcall fsgsbase bmi1 avx2 smep bmi2
erms invpcid cqm rdt_a avx512f avx512dq rdseed adx smap avx512ifma clflushopt clwb
avx512cd sha_ni avx512bw avx512vl xsaveopt xsavec xgetbv1 xsaves cqm_llc
cqm_occup_llc cqm_mbm_total cqm_mbm_local avx512_bf16 clzero irperf xsaveerptr rdpru
wbnoinvd amd_ppin cppc arat npt lbrv svm_lock nrip_save tsc_scale vmcb_clean
flushbyasid decodeassists pausefilter pfthreshold avic v_vmsave_vmload vgif
v_spec_ctrl avx512vbmi umip pku ospke avx512_vbmi2 gfni vaes vpclmulqdq avx512_vnni
avx512_bitalg avx512_vpopcntdq la57 rdpid overflow_recov succor smca fsrm flush_lld
Virtualization:              AMD-V
L1d cache:                    4 MiB (128 instances)
L1i cache:                    4 MiB (128 instances)
L2 cache:                     128 MiB (128 instances)
L3 cache:                     256 MiB (16 instances)
NUMA node(s):                 1
NUMA node0 CPU(s):           0-255
Vulnerability Itlb multihit:  Not affected
Vulnerability L1tf:           Not affected
Vulnerability Mds:            Not affected
Vulnerability Meltdown:       Not affected
Vulnerability Mmio stale data: Not affected
Vulnerability Retbleed:       Not affected
Vulnerability Spec store bypass: Mitigation; Speculative Store Bypass disabled via
prctl and seccomp
Vulnerability Spectre v1:      Mitigation; usercopy/swaps barriers and __user
pointer sanitization
Vulnerability Spectre v2:      Mitigation; Retpolines, IBPB conditional, IBRS_FW,
STIBP always-on, RSB filling, PBRSE-eIBRS Not affected
Vulnerability Srbds:          Not affected
Vulnerability Tsx async abort: Not affected

```

From lscpu --cache:

NAME	ONE-SIZE	ALL-SIZE	WAYS	TYPE	LEVEL	SETS	PHY-LINE	COHERENCY-SIZE
L1d	32K	4M	8	Data	1	64	1	64
L1i	32K	4M	8	Instruction	1	64	1	64
L2	1M	128M	8	Unified	2	2048	1	64
L3	16M	256M	16	Unified	3	16384	1	64

/proc/cpuinfo cache data

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Platform Notes (Continued)

cache size : 1024 KB

From numactl --hardware

WARNING: a numactl 'node' might or might not correspond to a physical chip.

available: 1 nodes (0)

```
node 0 cpus: 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27
28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50 51 52 53 54 55 56
57 58 59 60 61 62 63 64 65 66 67 68 69 70 71 72 73 74 75 76 77 78 79 80 81 82 83 84 85
86 87 88 89 90 91 92 93 94 95 96 97 98 99 100 101 102 103 104 105 106 107 108 109 110
111 112 113 114 115 116 117 118 119 120 121 122 123 124 125 126 127 128 129 130 131 132
133 134 135 136 137 138 139 140 141 142 143 144 145 146 147 148 149 150 151 152 153 154
155 156 157 158 159 160 161 162 163 164 165 166 167 168 169 170 171 172 173 174 175 176
177 178 179 180 181 182 183 184 185 186 187 188 189 190 191 192 193 194 195 196 197 198
199 200 201 202 203 204 205 206 207 208 209 210 211 212 213 214 215 216 217 218 219 220
221 222 223 224 225 226 227 228 229 230 231 232 233 234 235 236 237 238 239 240 241 242
243 244 245 246 247 248 249 250 251 252 253 254 255
```

node 0 size: 773242 MB

node 0 free: 771830 MB

node distances:

```
node 0
0: 10
```

From /proc/meminfo

```
MemTotal: 791800784 kB
HugePages_Total: 0
Hugepagesize: 2048 kB
```

/sys/devices/system/cpu/cpu*/cpufreq/scaling_governor has
performance

From /etc/*release* /etc/*version*

```
os-release:
NAME="SLES"
VERSION="15-SP5"
VERSION_ID="15.5"
PRETTY_NAME="SUSE Linux Enterprise Server 15 SP5"
ID="sles"
ID_LIKE="suse"
ANSI_COLOR="0;32"
CPE_NAME="cpe:/o:suse:sles:15:sp5"
```

uname -a:

```
Linux localhost 5.14.21-150500.53-default #1 SMP PREEMPT_DYNAMIC Wed May 10 07:56:26
UTC 2023 (b630043) x86_64 x86_64 x86_64 GNU/Linux
```

Kernel self-reported vulnerability status:

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Platform Notes (Continued)

CVE-2018-12207 (iTLB Multihit):	Not affected
CVE-2018-3620 (L1 Terminal Fault):	Not affected
Microarchitectural Data Sampling:	Not affected
CVE-2017-5754 (Meltdown):	Not affected
mmio_stale_data:	Not affected
retbleed:	Not affected
CVE-2018-3639 (Speculative Store Bypass):	Mitigation: Speculative Store Bypass disabled via prctl and seccomp
CVE-2017-5753 (Spectre variant 1):	Mitigation: usercopy/swaps barriers and __user pointer sanitization
CVE-2017-5715 (Spectre variant 2):	Mitigation: Retpolines, IBPB: conditional, IBRS_FW, STIBP: always-on, RSB filling, PBRSE-eIBRS: Not affected
CVE-2020-0543 (Special Register Buffer Data Sampling):	Not affected
CVE-2019-11135 (TSX Asynchronous Abort):	Not affected

run-level 3 May 13 01:31

```
SPEC is set to: /home/specaccel
Filesystem      Type  Size  Used Avail Use% Mounted on
/dev/sdb2       xfs   223G  174G   50G   78% /
```

```
From /sys/devices/virtual/dmi/id
Vendor:          Cisco Systems Inc
Product:         UCSC-C245-M8SX
Serial:          WZP27520MSW
```

Additional information from dmidecode 3.4 follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

```
Memory:
12x 0xCE00 M321R8GA0PB0-CWMCH 64 GB 2 rank 5600, configured at 4800
```

```
BIOS:
BIOS Vendor:     Cisco Systems, Inc.
BIOS Version:    C245M8.4.3.4.255.0410240854
BIOS Date:       04/10/2024
BIOS Revision:   5.27
```

(End of data from sysinfo program)



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Compiler Version Notes

=====
C | 403.stencil(base) 404.lbm(base) 452.ep(base) 457.spC(base)
| 470.bt(base)
=====

Intel(R) oneAPI DPC++/C++ Compiler 2024.0.2 (2024.0.2.20231213)
Target: x86_64-unknown-linux-gnu
Thread model: posix
InstalledDir: /home/intel_tools/compiler/compiler/2024.0/bin/compiler
Configuration file:
/home/intel_tools/compiler/compiler/2024.0/bin/compiler/./icx.cfg
=====

=====
Fortran | 450.md(base) 455.seismic(base) 456.spF(base) 460.ilbdc(base)
| 463.swim(base)
=====

ifx (IFX) 2024.0.2 20231213
Copyright (C) 1985-2023 Intel Corporation. All rights reserved.
=====

=====
Fortran, C | 453.clvrleaf(base) 459.miniGhost(base)
=====

ifx (IFX) 2024.0.2 20231213
Copyright (C) 1985-2023 Intel Corporation. All rights reserved.
Intel(R) oneAPI DPC++/C++ Compiler 2024.0.2 (2024.0.2.20231213)
Target: x86_64-unknown-linux-gnu
Thread model: posix
InstalledDir: /home/intel_tools/compiler/compiler/2024.0/bin/compiler
Configuration file:
/home/intel_tools/compiler/compiler/2024.0/bin/compiler/./icx.cfg
=====

Base Compiler Invocation

C benchmarks:
icx

Fortran benchmarks:
ifx

Benchmarks using both Fortran and C:
ifx icx



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Base Portability Flags

450.md: -80
457.spC: -Wl,--no-relax(icx)(*) -mcmmodel=medium -shared-intel
-Wl,--no-relax(icx)
459.miniGhost: -nofor-main

(*) Indicates a portability flag that was found in a non-portability variable.

Base Optimization Flags

C benchmarks:

-qopenmp -Ofast -O3 -march=common-avx512 -mprefer-vector-width=512
-qopt-multiple-gather-scatter-by-shuffles -flto -ffast-math
-qopt-dynamic-align -fvec-peel-loops -qopt-streaming-stores always
-Xclang -fopenmp-declare-target-scalar-defaultmap-firstprivate
-fimf-precision=low

Fortran benchmarks:

-qopenmp -Ofast -O3 -march=common-avx512 -mprefer-vector-width=512
-qopt-multiple-gather-scatter-by-shuffles -flto -ffast-math
-qopt-dynamic-align -fvec-peel-loops -qopt-streaming-stores always
-nostandard-realloc-lhs -align array32byte -auto
-fimf-accuracy-bits-sqrt=14 -fimf-precision=low

Benchmarks using both Fortran and C:

-qopenmp -Ofast -O3 -march=common-avx512 -mprefer-vector-width=512
-qopt-multiple-gather-scatter-by-shuffles -flto -ffast-math
-qopt-dynamic-align -fvec-peel-loops -qopt-streaming-stores always
-Xclang -fopenmp-declare-target-scalar-defaultmap-firstprivate
-fimf-precision=low -nostandard-realloc-lhs -align array32byte -auto
-fimf-accuracy-bits-sqrt=14

The flags file that was used to format this result can be browsed at

http://www.spec.org/accel2023/flags/Intel_compiler_flags_accel.2024.2024-05-29.html

You can also download the XML flags source by saving the following link:

http://www.spec.org/accel2023/flags/Intel_compiler_flags_accel.2024.2024-05-29.xml



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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

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