



SPEC® CINT2006 Result

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IBM Corporation

SPECint®_rate2006 = Not Run

IBM BladeCenter HS21 XM (Intel Xeon E5420)

SPECint_rate_base2006 = 98.6

CPU2006 license: 11

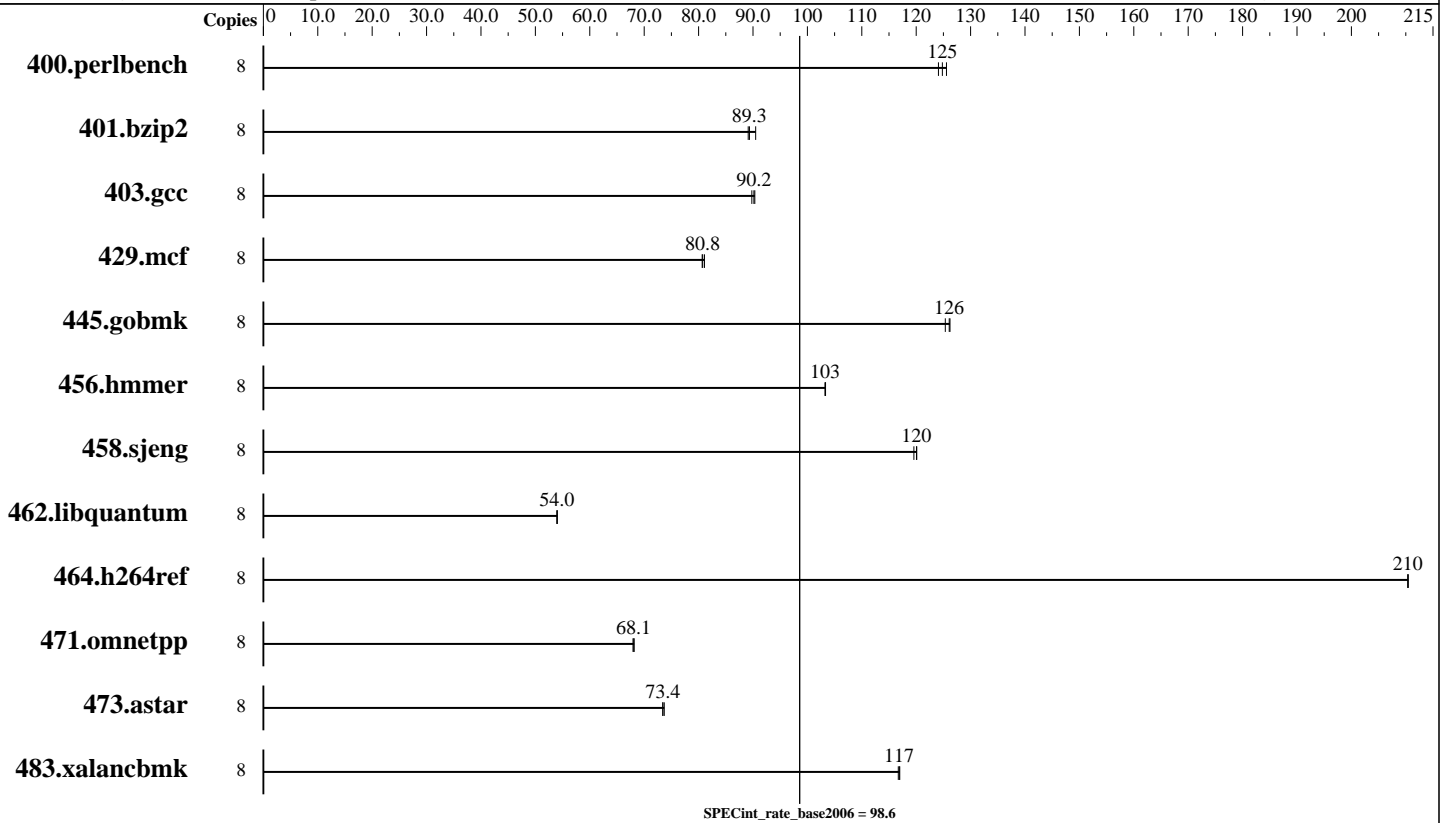
Test sponsor: IBM Corporation

Tested by: IBM Corporation

Test date: Dec-2007

Hardware Availability: Jan-2008

Software Availability: Nov-2007



Hardware

CPU Name: Intel Xeon E5420
 CPU Characteristics: 1333MHz system bus
 CPU MHz: 2500
 FPU: Integrated
 CPU(s) enabled: 8 cores, 2 chips, 4 cores/chip
 CPU(s) orderable: 1,2 chips
 Primary Cache: 32 KB I + 32 KB D on chip per core
 Secondary Cache: 12 MB I+D on chip per chip, 6 MB shared / 2 cores
 L3 Cache: None
 Other Cache: None
 Memory: 16 GB (8 x 2 GB DDR2-5300F ECC)
 Disk Subsystem: 1 x 36 GB SAS, 10000 RPM
 Other Hardware: None

Software

Operating System: SuSE Linux Enterprise Server 10 (x86_64), Kernel 2.6.16.21-0.8-smp
 Compiler: Intel C++ Compiler 10.1 for Linux Build 20070913 Package ID: l_cc_p_10.1.008
 Auto Parallel: No
 File System: ReiserFS
 System State: Multi-user, run level 3
 Base Pointers: 32-bit
 Peak Pointers: Not Applicable
 Other Software: MicroQuill SmartHeap 8.1 Binutils 2.17.50.0.15



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Results Table

Benchmark	Base						Peak							
	Copies	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio	Copies	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio
400.perlbench	8	622	126	626	125	630	124							
401.bzip2	8	853	90.5	866	89.1	864	89.3							
403.gcc	8	714	90.2	713	90.3	717	89.8							
429.mcf	8	900	81.1	903	80.8	905	80.7							
445.gobmk	8	666	126	669	125	665	126							
456.hammer	8	723	103	722	103	723	103							
458.sjeng	8	810	120	806	120	806	120							
462.libquantum	8	3070	54.0	3070	54.0	3070	54.0							
464.h264ref	8	841	210	841	210	842	210							
471.omnetpp	8	736	67.9	734	68.1	734	68.1							
473.astar	8	765	73.4	765	73.4	762	73.7							
483.xalancbmk	8	472	117	473	117	472	117							

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

General Notes

All benchmarks compiled in 32-bit mode
Hardware Sector Prefetch Disabled and Adjacent Sector Prefetch Disabled
taskset utility used to bind CPU(s) to processes

Base Compiler Invocation

C benchmarks:
icc

C++ benchmarks:
icpc

Base Portability Flags

400.perlbench: -DSPEC_CPU_LINUX_IA32
462.libquantum: -DSPEC_CPU_LINUX
483.xalancbmk: -DSPEC_CPU_LINUX

Base Optimization Flags

C benchmarks:
-fast -inline-calloc -opt-malloc-options=3

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Base Optimization Flags (Continued)

C++ benchmarks:

```
-xT -ipo -O3 -no-prec-div -Wl,-z,muldefs  
-L/spec/users/rahul/cpu2006.1.0/lib -lsmartheap
```

Base Other Flags

C benchmarks:

```
403.gcc: -Dalloca=_alloca
```

The flags file that was used to format this result can be browsed at

<http://www.spec.org/cpu2006/flags/Intel-ic10-ia32-intel64-linux-flags.20090714.13.html>

You can also download the XML flags source by saving the following link:

<http://www.spec.org/cpu2006/flags/Intel-ic10-ia32-intel64-linux-flags.20090714.13.xml>

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For questions about this result, please contact the tester.
For other inquiries, please contact webmaster@spec.org.

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