



SPEC® CFP2006 Result

Copyright 2006-2017 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS C480 M5 (Intel Xeon Platinum 8176
2.10GHz)

SPECfp®2006 = 148

SPECfp_base2006 = 140

CPU2006 license: 9019

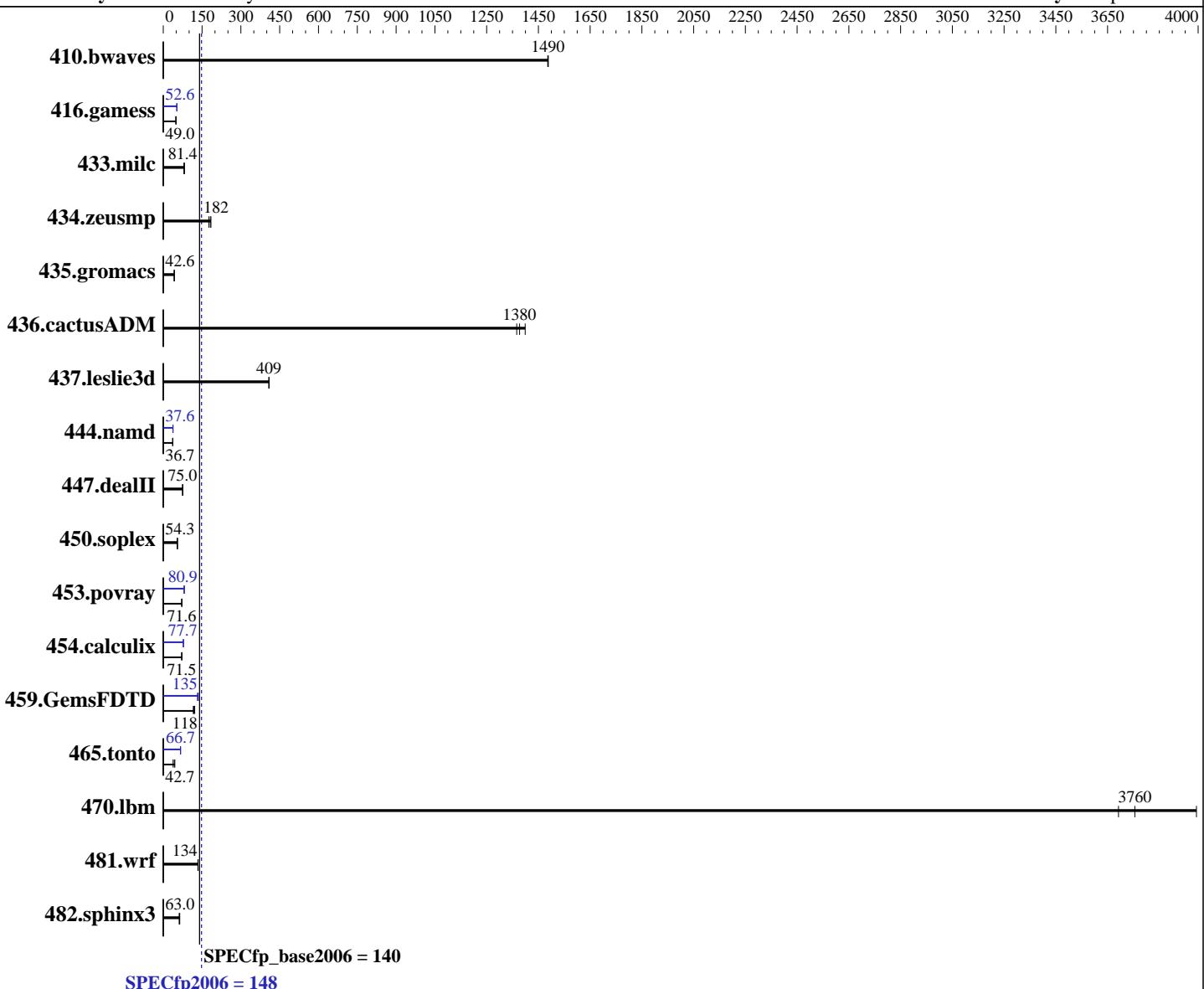
Test sponsor: Cisco Systems

Tested by: Cisco Systems

Test date: Aug-2017

Hardware Availability: Aug-2017

Software Availability: Apr-2017



Hardware

CPU Name: Intel Xeon Platinum 8176
 CPU Characteristics: Intel Turbo Boost Technology up to 3.80 GHz
 CPU MHz: 2100
 FPU: Integrated
 CPU(s) enabled: 112 cores, 4 chips, 28 cores/chip
 CPU(s) orderable: 2,4 chips
 Primary Cache: 32 KB I + 32 KB D on chip per core
 Secondary Cache: 1 MB I+D on chip per core

Software

Operating System: SUSE Linux Enterprise Server 12 SP2 4.4.21-69-default
 Compiler: C/C++: Version 17.0.3.191 of Intel C/C++ Compiler for Linux;
 Fortran: Version 17.0.3.191 of Intel Fortran Compiler for Linux
 Auto Parallel: Yes
 File System: xfs
 System State: Run level 5 (multi-user)

Continued on next page

Continued on next page



SPEC CFP2006 Result

Copyright 2006-2017 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS C480 M5 (Intel Xeon Platinum 8176
2.10GHz)

SPECfp2006 =

148

SPECfp_base2006 =

140

CPU2006 license: 9019

Test date: Aug-2017

Test sponsor: Cisco Systems

Hardware Availability: Aug-2017

Tested by: Cisco Systems

Software Availability: Apr-2017

Base Portability Flags

410.bwaves: -DSPEC_CPU_LP64
416.gamess: -DSPEC_CPU_LP64
433.milc: -DSPEC_CPU_LP64
434.zeusmp: -DSPEC_CPU_LP64
435.gromacs: -DSPEC_CPU_LP64 -nofor_main
436.cactusADM: -DSPEC_CPU_LP64 -nofor_main
437.leslie3d: -DSPEC_CPU_LP64
444.namd: -DSPEC_CPU_LP64
447.dealII: -DSPEC_CPU_LP64
450.soplex: -DSPEC_CPU_LP64
453.povray: -DSPEC_CPU_LP64
454.calculix: -DSPEC_CPU_LP64 -nofor_main
459.GemsFDTD: -DSPEC_CPU_LP64
465.tonto: -DSPEC_CPU_LP64
470.lbm: -DSPEC_CPU_LP64
481.wrf: -DSPEC_CPU_LP64 -DSPEC_CPU_CASE_FLAG -DSPEC_CPU_LINUX
482.sphinx3: -DSPEC_CPU_LP64

Base Optimization Flags

C benchmarks:

-xCORE-AVX2 -ipo -O3 -no-prec-div -parallel -qopt-prefetch

C++ benchmarks:

-xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch

Fortran benchmarks:

-xCORE-AVX2 -ipo -O3 -no-prec-div -parallel -qopt-prefetch

Benchmarks using both Fortran and C:

-xCORE-AVX2 -ipo -O3 -no-prec-div -parallel -qopt-prefetch

Peak Compiler Invocation

C benchmarks:

icc -m64

C++ benchmarks:

icpc -m64

Fortran benchmarks:

ifort -m64

Benchmarks using both Fortran and C:

icc -m64 ifort -m64



SPEC CFP2006 Result

Copyright 2006-2017 Standard Performance Evaluation Corporation

Cisco Systems	SPECfp2006 =	148
Cisco UCS C480 M5 (Intel Xeon Platinum 8176 2.10GHz)	SPECfp_base2006 =	140
CPU2006 license: 9019	Test date:	Aug-2017
Test sponsor: Cisco Systems	Hardware Availability:	Aug-2017
Tested by: Cisco Systems	Software Availability:	Apr-2017

Peak Optimization Flags (Continued)

Benchmarks using both Fortran and C:

435.gromacs: basepeak = yes

436.cactusADM: basepeak = yes

454.calculix: -xCORE-AVX2 -ipo -O3 -no-prec-div -auto-ilp32

481.wrf: basepeak = yes

The flags files that were used to format this result can be browsed at

<http://www.spec.org/cpu2006/flags/Intel-ic17.0-official-linux64-revF.html>
<http://www.spec.org/cpu2006/flags/Cisco-Platform-Settings-V1.2-revH.html>

You can also download the XML flags sources by saving the following links:

<http://www.spec.org/cpu2006/flags/Intel-ic17.0-official-linux64-revF.xml>
<http://www.spec.org/cpu2006/flags/Cisco-Platform-Settings-V1.2-revH.xml>

SPEC and SPECfp are registered trademarks of the Standard Performance Evaluation Corporation. All other brand and product names appearing in this result are trademarks or registered trademarks of their respective holders.

For questions about this result, please contact the tester.
For other inquiries, please contact webmaster@spec.org.

Tested with SPEC CPU2006 v1.2.

Report generated on Wed Sep 6 11:46:31 2017 by SPEC CPU2006 PS/PDF formatter v6932.
Originally published on 5 September 2017.