



SPEC CPU®2017 Integer Speed Result

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Cisco Systems

Cisco UCS C240 M5 (Intel Xeon Gold 6146,
3.20GHz)

SPECspeed®2017_int_base = 9.79

SPECspeed®2017_int_peak = Not Run

CPU2017 License: 9019

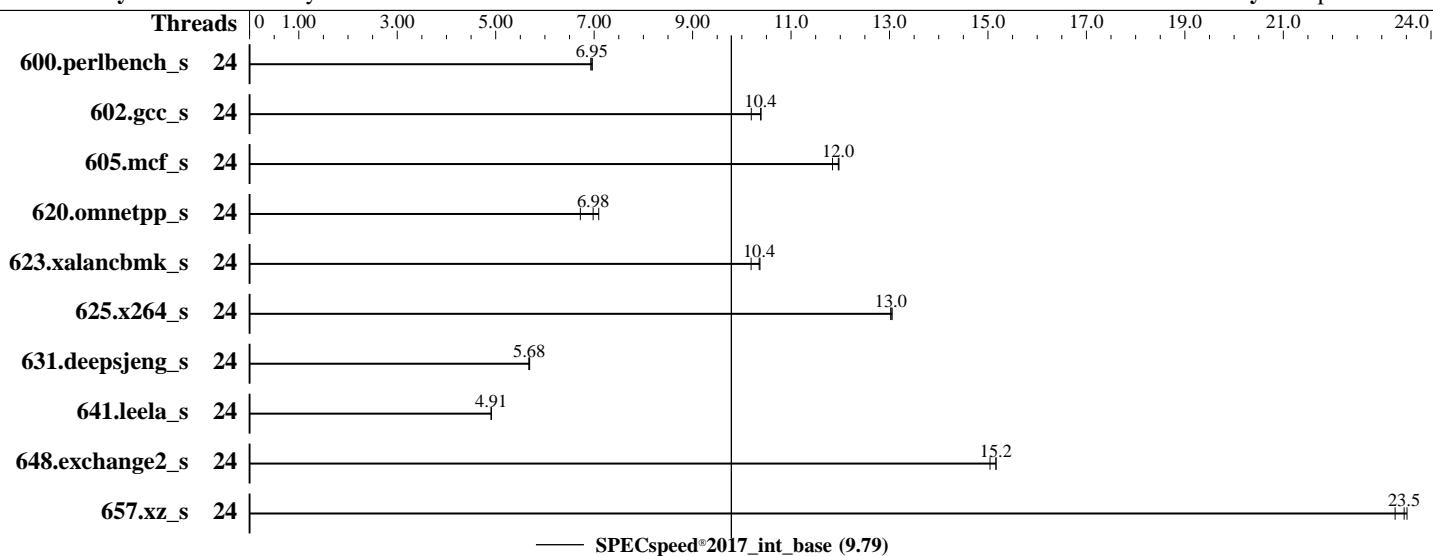
Test Sponsor: Cisco Systems

Tested by: Cisco Systems

Test Date: Oct-2017

Hardware Availability: Oct-2017

Software Availability: Sep-2017



Hardware

CPU Name: Intel Xeon Gold 6146
 Max MHz: 4200
 Nominal: 3200
 Enabled: 24 cores, 2 chips
 Orderable: 1,2 Chips
 Cache L1: 32 KB I + 32 KB D on chip per core
 L2: 1 MB I+D on chip per core
 L3: 24.75 MB I+D on chip per chip
 Other: None
 Memory: 384 GB (24 x 16 GB 2Rx4 PC4-2666V-R)
 Storage: 1 x 800 GB SSD SAS
 Other: None

Software

OS: SUSE Linux Enterprise Server 12 SP2 (x86_64)
 4.4.21-69-default
 Compiler: C/C++: Version 18.0.0.128 of Intel C/C++
 Compiler for Linux;
 Fortran: Version 18.0.0.128 of Intel Fortran
 Compiler for Linux
 Parallel: Yes
 Firmware: Version 3.1.1d released Jun-2017
 File System: xfs
 System State: Run level 3 (multi-user)
 Base Pointers: 64-bit
 Peak Pointers: Not Applicable
 Other: jemalloc: jemalloc memory allocator library
 V5.0.1;
 jemalloc: configured and built at default for
 32bit (i686) and 64bit (x86_64) targets
 Power Management: --



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Results Table

Benchmark	Base								Peak							
	Threads	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio	Threads	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio
600.perlbench_s	24	255	6.96	<u>255</u>	<u>6.95</u>	256	6.93									
602.gcc_s	24	383	10.4	391	10.2	<u>384</u>	<u>10.4</u>									
605.mcf_s	24	394	12.0	399	11.8	<u>395</u>	<u>12.0</u>									
620.omnetpp_s	24	243	6.72	<u>234</u>	<u>6.98</u>	230	7.09									
623.xalancbmk_s	24	139	10.2	137	10.4	<u>137</u>	<u>10.4</u>									
625.x264_s	24	135	13.1	135	13.0	<u>135</u>	<u>13.0</u>									
631.deepsjeng_s	24	252	5.69	253	5.67	<u>252</u>	<u>5.68</u>									
641.leela_s	24	<u>347</u>	<u>4.91</u>	347	4.91	348	4.91									
648.exchange2_s	24	194	15.2	195	15.0	<u>194</u>	<u>15.2</u>									
657.xz_s	24	266	23.3	263	23.5	<u>264</u>	<u>23.5</u>									

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Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

General Notes

Environment variables set by runcpu before the start of the run:

KMP_AFFINITY = "granularity=fine,scatter"

LD_LIBRARY_PATH = "/home/cpu2017/lib/ia32:/home/cpu2017/lib/intel64:/home/cpu2017/je5.0.1-32:/home/cpu2017/je5.0.1-64"

OMP_STACKSIZE = "702M"

Binaries compiled on a system with 1x Intel Core i7-4790 CPU + 32GB RAM
memory using Redhat Enterprise Linux 7.4

Transparent Huge Pages enabled by default

Prior to runcpu invocation

Filesystem page cache synced and cleared with:

```
sync; echo 3> /proc/sys/vm/drop_caches
jemalloc, a general purpose malloc implementation
```

built with the RedHat Enterprise 7.4, and the system compiler gcc 4.8.5
sources available from jemalloc.net or <https://github.com/jemalloc/jemalloc/releases>

Platform Notes

BIOS Settings:

Intel HyperThreading Technology set to Disabled

CPU performance set to Enterprise

Power Performance Tuning set to OS

SNC set to Disabled

IMC Interleaving set to Auto

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Platform Notes (Continued)

Patrol Scrub set to Disabled

Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r5797 of 2017-06-14 96c45e4568ad54c135fd618bcc091c0f
running on linux-nvug Fri Oct 13 19:51:29 2017

SUT (System Under Test) info as seen by some common utilities.

For more information on this section, see

<https://www.spec.org/cpu2017/Docs/config.html#sysinfo>

From /proc/cpuinfo

```
model name : Intel(R) Xeon(R) Gold 6146 CPU @ 3.20GHz
  2 "physical id"s (chips)
  24 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following
excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
  cpu cores : 12
  siblings   : 12
  physical 0: cores 0 1 2 3 8 9 10 11 18 19 24 27
  physical 1: cores 0 1 2 3 4 9 10 16 18 19 25 26
```

From lscpu:

```
Architecture:           x86_64
CPU op-mode(s):        32-bit, 64-bit
Byte Order:            Little Endian
CPU(s):                24
On-line CPU(s) list:  0-23
Thread(s) per core:   1
Core(s) per socket:   12
Socket(s):             2
NUMA node(s):          2
Vendor ID:             GenuineIntel
CPU family:            6
Model:                 85
Model name:            Intel(R) Xeon(R) Gold 6146 CPU @ 3.20GHz
Stepping:               4
CPU MHz:                3023.513
CPU max MHz:           4200.0000
CPU min MHz:           1200.0000
BogoMIPS:              6384.98
Virtualization:        VT-x
L1d cache:              32K
L1i cache:              32K
L2 cache:                1024K
L3 cache:                25344K
NUMA node0 CPU(s):     0-11
NUMA node1 CPU(s):     12-23
Flags:                  fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
```

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Platform Notes (Continued)

```
pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp
lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc
aperfmpfperf eagerfpu pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg
fma cx16 xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes
xsave avx f16c rdrand lahf_lm abm 3dnowprefetch ida arat epb pln pts dtherm hwp
hwp_act_window hwp_epp hwp_pkg_req intel_pt tpr_shadow vmmi flexpriority ept vpid
fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 erms invpcid rtm cqm mpx avx512f
avx512dq rdseed adx smap clflushopt clwb avx512cd avx512bw avx512vl xsaveopt xsavec
xgetbv1 cqmq_llc cqmq_occrap_llc
```

```
/proc/cpuinfo cache data
cache size : 25344 KB
```

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a physical chip.

```
available: 2 nodes (0-1)
node 0 cpus: 0 1 2 3 4 5 6 7 8 9 10 11
node 0 size: 192090 MB
node 0 free: 191402 MB
node 1 cpus: 12 13 14 15 16 17 18 19 20 21 22 23
node 1 size: 193518 MB
node 1 free: 192918 MB
node distances:
node 0 1
 0: 10 21
 1: 21 10
```

From /proc/meminfo

```
MemTotal:      394863424 kB
HugePages_Total:       0
Hugepagesize:     2048 kB
```

From /etc/*release* /etc/*version*

```
SuSE-release:
  SUSE Linux Enterprise Server 12 (x86_64)
  VERSION = 12
  PATCHLEVEL = 2
  # This file is deprecated and will be removed in a future service pack or release.
  # Please check /etc/os-release for details about this release.
os-release:
  NAME="SLES"
  VERSION="12-SP2"
  VERSION_ID="12.2"
  PRETTY_NAME="SUSE Linux Enterprise Server 12 SP2"
  ID="sles"
  ANSI_COLOR="0;32"
  CPE_NAME="cpe:/o:suse:sles:12:sp2"
```

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Platform Notes (Continued)

uname -a:

```
Linux linux-nvug 4.4.21-69-default #1 SMP Tue Oct 25 10:58:20 UTC 2016 (9464f67)
x86_64 x86_64 x86_64 GNU/Linux
```

run-level 3 Oct 13 19:50

SPEC is set to: /home/cpu2017

Filesystem	Type	Size	Used	Avail	Use%	Mounted on
/dev/sda2	xfs	644G	138G	507G	22%	/

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

BIOS Cisco Systems, Inc. C240M5.3.1.1d.0.0615170707 06/15/2017

Memory:

24x 0xCE00 M393A2G40EB2-CTD 16 GB 2 rank 2666

(End of data from sysinfo program)

Compiler Version Notes

=====

C | 600.perlbench_s(base) 602.gcc_s(base) 605.mcf_s(base)
| 625.x264_s(base) 657.xz_s(base)

=====
icc (ICC) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation. All rights reserved.
=====

=====
C++ | 620.omnetpp_s(base) 623.xalancbmk_s(base) 631.deepsjeng_s(base)
| 641.leela_s(base)

=====
icpc (ICC) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation. All rights reserved.
=====

=====
Fortran | 648.exchange2_s(base)

=====
ifort (IFORT) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation. All rights reserved.
=====



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Base Compiler Invocation

C benchmarks:

icc

C++ benchmarks:

icpc

Fortran benchmarks:

ifort

Base Portability Flags

600.perlbench_s: -DSPEC_LP64 -DSPEC_LINUX_X64
602.gcc_s: -DSPEC_LP64
605.mcf_s: -DSPEC_LP64
620.omnetpp_s: -DSPEC_LP64
623.xalancbmk_s: -DSPEC_LP64 -DSPEC_LINUX
625.x264_s: -DSPEC_LP64
631.deepsjeng_s: -DSPEC_LP64
641.leela_s: -DSPEC_LP64
648.exchange2_s: -DSPEC_LP64
657.xz_s: -DSPEC_LP64

Base Optimization Flags

C benchmarks:

-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=3 -qopenmp -DSPEC_OPENMP
-L/usr/local/je5.0.1-64/lib -ljemalloc

C++ benchmarks:

-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=3 -L/usr/local/je5.0.1-64/lib -ljemalloc

Fortran benchmarks:

-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=3 -nostandard-realloc-lhs -align array32byte
-L/usr/local/je5.0.1-64/lib -ljemalloc



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Base Other Flags

C benchmarks:

-m64 -std=c11

C++ benchmarks:

-m64

Fortran benchmarks:

-m64

The flags files that were used to format this result can be browsed at

<http://www.spec.org/cpu2017/flags/Intel-ic18.0-official-linux64.html>

<http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.2-revH.html>

You can also download the XML flags sources by saving the following links:

<http://www.spec.org/cpu2017/flags/Intel-ic18.0-official-linux64.xml>

<http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.2-revH.xml>

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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

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